240pin Unbuffered DDR2 SDRAM MODULE

Based on 128Mx8 DDR2 SDRAM G-die

Features

Performance:

		PC2-6400	Unit
Speed Sort		-AC	
DIMM $\overline{CAS}$ Latency*		5	
f_{CK}	Clock Frequency	400	MHz
t_{CK}	Clock Cycle	2.5	ns
f_{DQ}	DQ Burst Frequency	800	Mbps

- JEDEC Standard 240-pin Dual In-Line Memory Module
- 128Mx64 and 256Mx64 DDR2 Unbuffered DIMM based on Elixir 128Mx8 DDR2 SDRAM G-die component
- Double Data Rate architecture; two data transfer per clock cycle
- Differential bi-directional data strobe (DQS & $\overline{DQS}$)
- DQS is edge-aligned with data for reads and is center-aligned with data for writes
- Differential clock inputs (CK & $\overline{CK}$)
- Intended for 400MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{DD} = V_{DDQ} = 1.8V \pm 0.1V$
- 7.8 µs Max. Average Periodic Refresh Interval
- Programmable Operation:
  - Device $\overline{CAS}$ Latency: 5
  - Burst Length: 4, 8
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 14/10/1 Addressing (row/column/rank) – 1GB
- 14/10/2 Addressing (row/column/rank) – 2GB
- Serial Presence Detect
- On Die Termination (ODT)
- OCD impedance adjustment.
- Gold contacts
- SDRAMs in 60-ball BGA Package
- RoHs Compliance.

Description

M2Y(F)1G64TU88G7(4)B and M2Y(F)2G64TU8HG5(4)B are 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), organized as one rank 128Mx64 and two ranks 256Mx64 high-speed memory array.

M2Y(F)1G64TU88G7(4)B uses eight 128Mx8 DDR2 SDRAMs and M2Y(F)2G64TU8G5(4)B uses sixteen 128Mx8 DDR2 SDRAMs in BGA packages. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All Elixir DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

The DIMM is intended for use in applications operating up to 400MHz clock speeds and achieves high-speed data transfer rates of up to 800Mbps. Prior to any access operation, the device $\overline{CAS}$ latency and burst / length /operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0, BA1 and BA2 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Leads	Power	Note
M2Y1G64TU88G7B-AC	400MHz (2.50ns @ CL = 5)	DDR2-800	PC2-6400	128Mx64	GOLD	1.8V	Rohs compliance
M2F1G64TU88G4B-AC	400MHz (2.50ns @ CL = 5)	DDR2-800	PC2-6400				Rohs compliance and Halogen-Free
M2Y2G64TU8HG5B-AC	400MHz (2.50ns @ CL = 5)	DDR2-800	PC2-6400	256Mx64			Rohs compliance
M2F2G64TU8HG4B-AC	400MHz (2.50ns @ CL = 5)	DDR2-800	PC2-6400				Rohs compliance and Halogen-Free

Pin Description

CK0~CK2 $\overline{CK0}$~$\overline{CK2}$	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS8	Bidirectional data strobes
$\overline{RAS}$	Row Address Strobe	DM0-DM8	Input Data Mask
$\overline{CAS}$	Column Address Strobe	$\overline{DQS0}$-$\overline{DQS8}$	Differential data strobes
$\overline{WE}$	Write Enable	VDD	Power (1.8V)
$\overline{CS0}$, $\overline{CS1}$	Chip Selects	VREF	Ref. Voltage for SSTL_18 inputs
A0-A9, A0-A13	Address Inputs	VDDSPD	Serial EEPROM positive power supply
A10/AP	Column Address Input/Auto-precharge	VSS	Ground
BA0 ~ BA2	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RESET	Reset pin	SDA	Serial Presence Detect Data input/output
ODT0, ODT1	On-die termination control lines	SA0 ~ SA2	Serial Presence Detect Address Inputs
NC	No Connect		

Note: ODT1, CKE1 and $\overline{CS1}$ are only support in 2GB module type.

Pinout

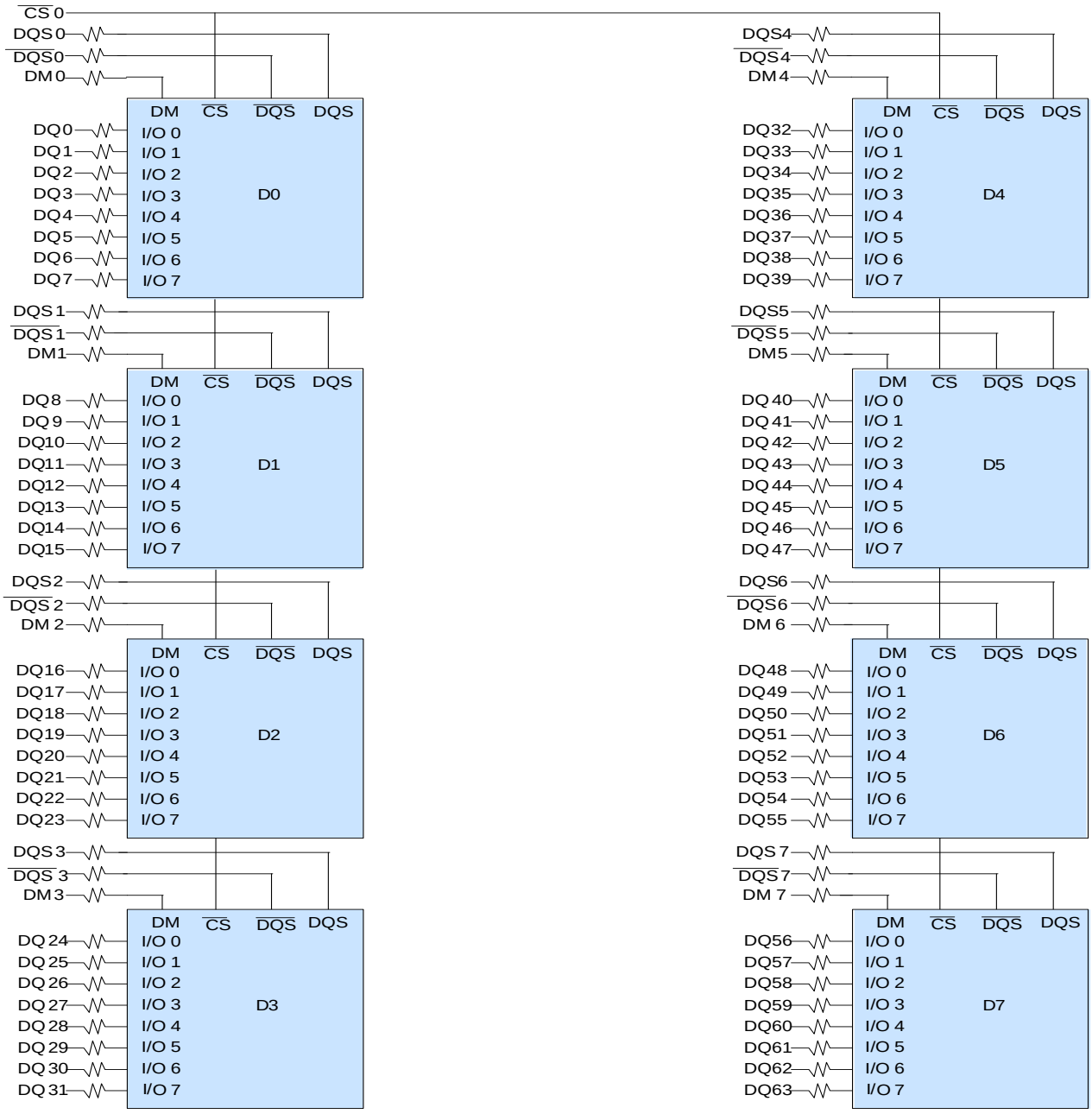
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V_{REF}	42	NC	82	V_{SS}	121	V_{SS}	162	NC	202	DM4
2	V_{SS}	43	NC	83	$\overline{DQS4}$	122	DQ4	163	V_{SS}	203	NC
3	DQ0	44	V_{SS}	84	DQS4	123	DQ5	164	NC	204	V_{SS}
4	DQ1	45	NC	85	V_{SS}	124	V_{SS}	165	NC	205	DQ38
5	V_{SS}	46	NC	86	DQ34	125	DM0	166	V_{SS}	206	DQ39
6	$\overline{DQS0}$	47	V_{SS}	87	DQ35	126	NC	167	NC	207	V_{SS}
7	DQS0	48	NC	88	V_{SS}	127	V_{SS}	168	NC	208	DQ44
8	V_{SS}	49	NC	89	DQ40	128	DQ6	169	V_{SS}	209	DQ45
9	DQ2	50	V_{SS}	90	DQ41	129	DQ7	170	V_{DDQ}	210	V_{SS}
10	DQ3	51	V_{DDQ}	91	V_{SS}	130	V_{SS}	171	NC,CKE1	211	DM5
11	V_{SS}	52	CKE0	92	$\overline{DQS5}$	131	DQ12	172	V_{DD}	212	NC
12	DQ8	53	V_{DD}	93	DQS5	132	DQ13	173	NC	213	V_{SS}
13	DQ9	54	BA2	94	V_{SS}	133	V_{SS}	174	NC	214	DQ46
14	V_{SS}	55	NC	95	DQ42	134	DM1	175	V_{DDQ}	215	DQ47
15	$\overline{DQS1}$	56	V_{DDQ}	96	DQ43	135	NC	176	A12	216	V_{SS}
16	DQS1	57	A11	97	V_{SS}	136	V_{SS}	177	A9	217	DQ52
17	V_{SS}	58	A7	98	DQ48	137	CK1	178	V_{DD}	218	DQ53
18	NC	59	V_{DD}	99	DQ49	138	$\overline{CK1}$	179	A8	219	V_{SS}
19	NC	60	A5	100	V_{SS}	139	V_{SS}	180	A6	220	CK2
20	V_{SS}	61	A4	101	SA2	140	DQ14	181	V_{DDQ}	221	$\overline{CK2}$
21	DQ10	62	V_{DDQ}	102	NC	141	DQ15	182	A3	222	V_{SS}
22	DQ11	63	A2	103	V_{SS}	142	V_{SS}	183	A1	223	DM6
23	V_{SS}	64	V_{DD}	104	$\overline{DQS6}$	143	DQ20	184	V_{DD}	224	NC
24	DQ16	KEY		105	DQS6	144	DQ21	KEY		225	V_{SS}
25	DQ17	65	V_{SS}	106	V_{SS}	145	V_{SS}	185	CK0	226	DQ54
26	V_{SS}	66	V_{SS}	107	DQ50	146	DM2	186	$\overline{CK0}$	227	DQ55
27	$\overline{DQS2}$	67	VDD	108	DQ51	147	NC	187	VDD	228	V_{SS}
28	DQS2	68	NC	109	V_{SS}	148	V_{SS}	188	A0	229	DQ60
29	V_{SS}	69	VDD	110	DQ56	149	DQ22	189	V_{DD}	230	DQ61
30	DQ18	70	A10/AP	111	DQ57	150	DQ23	190	BA1	231	V_{SS}
31	DQ19	71	BA0	112	V_{SS}	151	V_{SS}	191	V_{DDQ}	232	DM7
32	V_{SS}	72	VDDQ	113	$\overline{DQS7}$	152	DQ28	192	$\overline{RAS}$	233	NC
33	DQ24	73	$\overline{WE}$	114	DQS7	153	DQ29	193	$\overline{CS0}$	234	V_{SS}
34	DQ25	74	$\overline{CAS}$	115	V_{SS}	154	V_{SS}	194	V_{DDQ}	235	DQ62
35	V_{SS}	75	V_{DDQ}	116	DQ58	155	DM3	195	ODT0	236	DQ63
36	$\overline{DQS3}$	76	NC, $\overline{CS1}$	117	DQ59	156	NC	196	A13	237	V_{SS}
37	DQS3	77	NC,ODT1	118	V_{SS}	157	V_{SS}	197	V_{DD}	238	V_{DDSPD}
38	V_{SS}	78	V_{DDQ}	119	SDA	158	DQ30	198	V_{SS}	239	SA0
39	DQ26	79	V_{SS}	120	SCL	159	DQ31	199	DQ36	240	SA1
40	DQ27	80	DQ32			160	V_{SS}	200	DQ37		
41	V_{SS}	81	DQ33			161	NC	201	V_{SS}		

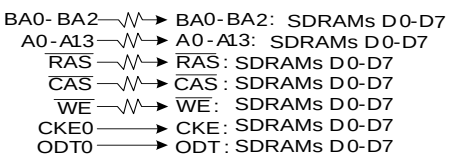
Note: 1. NC = No Connect.
2. $\overline{CS1}$, ODT1 and CKE1 (Pins 76, 77 and 171) are only support in 2GB module type.

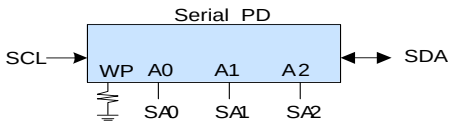
Input/Output Functional Description

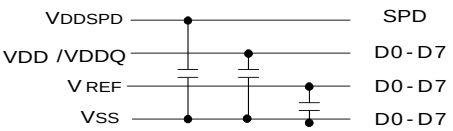
Symbol	Type	Polarity	Function
CK0, CK1, CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode. CKE1 apply on 2GB UDIMM only.
$\overline{CS0}$, $\overline{CS1}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. $\overline{CS1}$ apply on 2GB UDIMM only.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-18 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
ODT0, ODT1	Input	Active High	On-Die Termination control signals. ODT1 apply on 2GB UDIMM only.
BA0 – BA2	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11 - A13	(SSTL)	-	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke “Autoprecharge” operation at the end of the Burst Read or Write cycle. If AP is high, Autoprecharge’s selected and BA0/BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63	(SSTL)	Active High	Data and Check Bit Input /Output pins.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR2 SDRAM input buffers and core logic
DQS0 – DQS8 $\overline{DQS0}$ – $\overline{DQS8}$	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
SA0 – SA2		-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull-up.
V_{DDSPD}	Supply		Serial EEPROM positive power supply.

Functional Block Diagram (1GB, 1 Rank, 128Mx8 DDR2 SDRAMs)

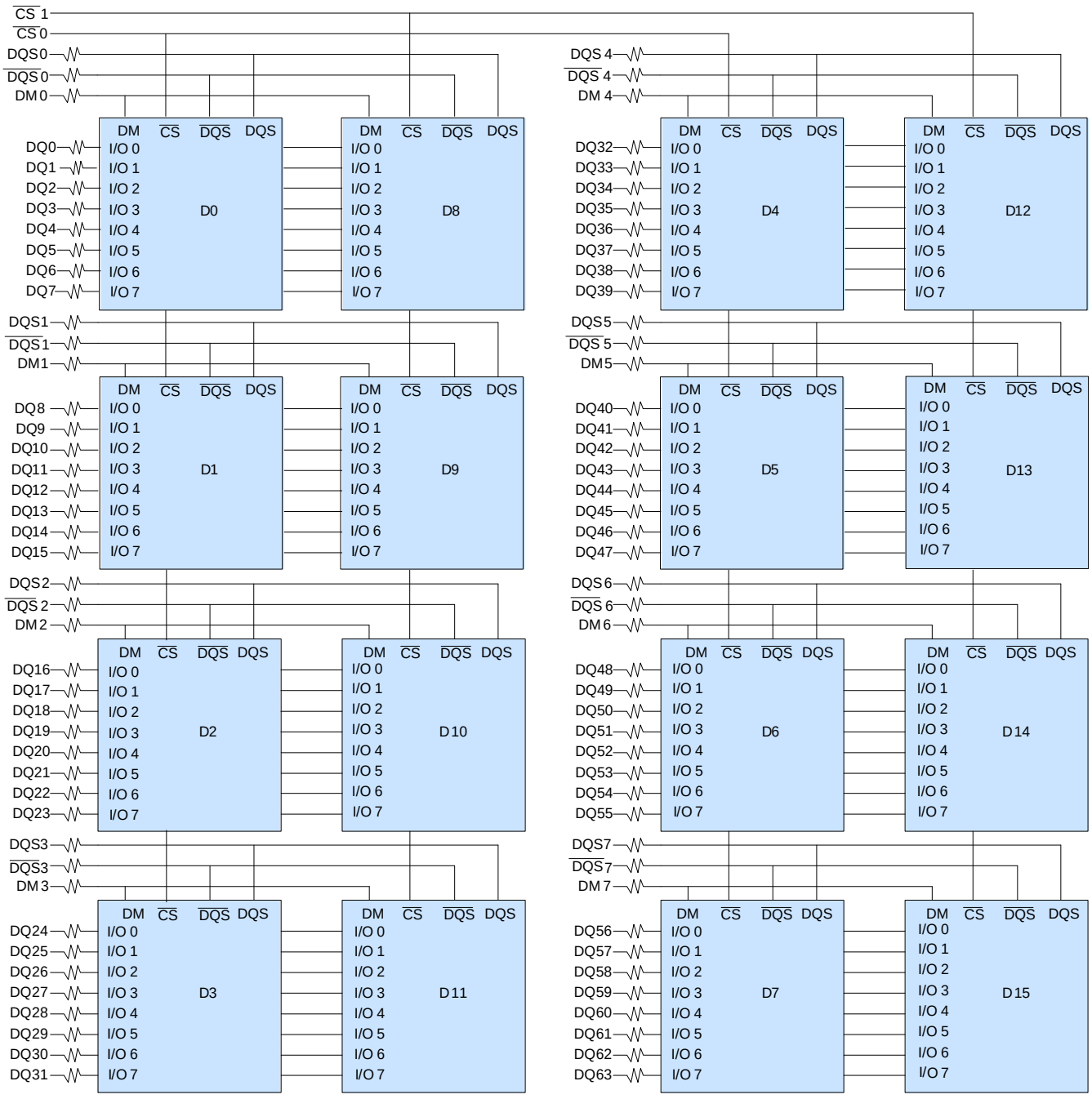


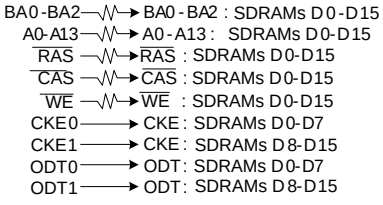


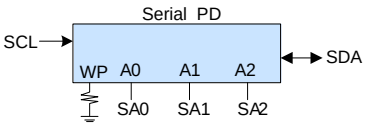


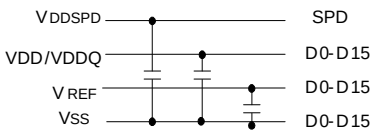


Functional Block Diagram (2GB, 2 Ranks, 128Mx8 DDR2 SDRAMs)









Serial Presence Detect (1GB – 1 Rank, DDR2 SDRAMs)

Serial Presence Detect [1GB –1 Rank, DDR2 SDRAMs]		
Byte	**Description**	**SPD Data Entry (Hex.)**
		-AC
0	Number of Serial PD Bytes Written during Production	80
1	Total Number of Bytes in Serial PD device	08
2	Fundamental Memory Type	08
3	Number of Row Addresses on Assembly	0E
4	Number of Column Addresses on Assembly	0A
5	Number of DIMM Ranks, Package, and Height	60
6	Data Width of Assembly	40
7	Reserved	00
8	Voltage Interface Level of this Assembly	05
9	DDR2 SDRAM Device Cycle Time at CL=5	25
10	DDR2 SDRAM Device Access Time (t_{ac}) from Clock at CL=5	40
11	DIMM Configuration Type	00
12	Refresh Rate/Type	82
13	Primary DDR2 SDRAM Width	08
14	Error Checking DDR2 SDRAM Device Width	00
15	Reserved	00
16	DDR2 SDRAM Device Attributes: Burst Length Supported	0C
17	DDR2 SDRAM Device Attributes: Number of Device Banks	08
18	DDR2 SDRAM Device Attributes: $\overline{CAS}$ Latencies Supported	38
19	DIMM Mechanical Characteristics	01
20	DDR2 SDRAM DIMM Type Information	02
21	DDR2 SDRAM Module Attributes	00
22	DDR2 SDRAM Device Attributes: General	03
23	Minimum Clock Cycle at CL=4	3D
24	Maximum Data Access Time from Clock at CL=4	50
25	Minimum Clock Cycle Time at CL=3	50
26	Maximum Data Access Time from Clock at CL=3	60
27	Minimum Row Precharge Time (t_{RP})	32
28	Minimum Row Active to Row Active delay (t_{RRD})	1E
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD})	32
30	Minimum Active to Precharge Time (t_{RAS})	2D
31	Module Rank Density	01
32	Address and Command Setup Time Before Clock (t_{IS})	17
33	Address and Command Hold Time After Clock (t_{IH})	25
34	Data Input Setup Time Before Clock (t_{DS})	05
35	Data Input Hold Time After Clock (tDH)	12
36	Write Recovery Time (t_{WR})	3C
37	Internal Write to Read Command delay (t_{WTR})	1E
38	Internal Read to Precharge delay (t_{RTP})	1E
39	Reserved	00
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	36
41	Minimum Core Cycle Time (t_{RC})	39
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	7F
43	Maximum Clock Cycle Time (t_{CK})	80
44	Max. DQS-DQ Skew Factor (tQHS)	14
45	Read Data Hold Skew Factor (tQHS)	1E
46-61	Reserved	--
62	SPD Reversion	13
63	Checksum for Byte 0-62	F9
64-71	Manufacturer's JEDEC ID Code	--
72	Module Manufacturing Location	00
73-91	Module Part number	--
92-255	Reserved	--

Serial Presence Detect (2GB – 2 Ranks, DDR2 SDRAMs)

Serial Presence Detect [2GB – 2 Ranks, DDR2 SDRAMs]		
Byte	Description	SPD Data Entry (Hex.)
		-AC
0	Number of Serial PD Bytes Written during Production	80
1	Total Number of Bytes in Serial PD device	08
2	Fundamental Memory Type	08
3	Number of Row Addresses on Assembly	0E
4	Number of Column Addresses on Assembly	0A
5	Number of DIMM Ranks, Package, and Height	61
6	Data Width of Assembly	40
7	Reserved	00
8	Voltage Interface Level of this Assembly	05
9	DDR2 SDRAM Device Cycle Time at CL=5	25
10	DDR2 SDRAM Device Access Time (t_{ac}) from Clock at CL=5	40
11	DIMM Configuration Type	00
12	Refresh Rate/Type	82
13	Primary DDR2 SDRAM Width	08
14	Error Checking DDR2 SDRAM Device Width	00
15	Reserved	00
16	DDR2 SDRAM Device Attributes: Burst Length Supported	0C
17	DDR2 SDRAM Device Attributes: Number of Device Banks	08
18	DDR2 SDRAM Device Attributes: $\overline{CAS}$ Latencies Supported	38
19	DIMM Mechanical Characteristics	01
20	DDR2 SDRAM DIMM Type Information	02
21	DDR2 SDRAM Module Attributes	00
22	DDR2 SDRAM Device Attributes: General	03
23	Minimum Clock Cycle at CL=4	3D
24	Maximum Data Access Time from Clock at CL=4	50
25	Minimum Clock Cycle Time at CL=3	50
26	Maximum Data Access Time from Clock at CL=3	60
27	Minimum Row Precharge Time (t_{RP})	32
28	Minimum Row Active to Row Active delay (t_{RRD})	1E
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD})	32
30	Minimum Active to Precharge Time (t_{RAS})	2D
31	Module Rank Density	01
32	Address and Command Setup Time Before Clock (t_{IS})	17
33	Address and Command Hold Time After Clock (t_{IH})	25
34	Data Input Setup Time Before Clock (t_{DS})	05
35	Data Input Hold Time After Clock (tDH)	12
36	Write Recovery Time (t_{WR})	3C
37	Internal Write to Read Command delay (t_{WTR})	1E
38	Internal Read to Precharge delay (t_{RTP})	1E
39	Reserved	00
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	36
41	Minimum Core Cycle Time (t_{RC})	39
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	7F
43	Maximum Clock Cycle Time (t_{CK})	80
44	Max. DQS-DQ Skew Factor (tQHS)	14
45	Read Data Hold Skew Factor (tQHS)	1E
46-61	Reserved	--
62	SPD Reversion	13
63	Checksum for Byte 0-62	FA
64-71	Manufacturer's JEDEC ID Code	--
72	Module Manufacturing Location	00
73-91	Module Part number	--
92-255	Reserved	--

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.5 to 2.3	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to Vss	-0.5 to 2.3	V
V_{DDQL}	Voltage on V_{DDQL} supply relative to Vss	-0.5 to 2.3	V
V_{DD}	Voltage on VDD supply relative to Vss	-1.0 to +2.3	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Operating Conditions

Symbol	Parameter	Rating	Units	Note
T_{CASE}	Operating Temperature (Ambient)	0 to 95	°C	1,2,3
T_{STG}	Storage Temperature (Plastic)	-55 to 100	°C	
I_L	Short Circuit Output Current	-5 to 5	Ma	

Note:
1. Case temperature is measured at top and center side of any DRAMs.
2. t_{CASE} > 85°C ➔ t_{REFI} = 3.9 µs
3. All DRAM specification only support 0°C < t_{CASE} < 85°C

DC Electrical Characteristics and Operating Conditions

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	1.7	1.9	V	1
V_{DDQ}	Supply Voltage for Output	1.7	1.9	V	1, 3
V_{DDL}	Supply Voltage for V_{DDQL}	1.7	1.9	V	3
V_{REF}	Input Reference Voltage	0.49V_{DDQ}	0.51V_{DDQ}	Mv	2
V_{TT}	Termination Voltage	V_{REF} – 0.04	V_{REF} + 0.04	V	4
V_{IH} (DC)	Input High (Logic1) Voltage	V_{REF} + 0.125	V_{DDQ} + 0.3	V	
V_{IL} (DC)	Input Low (Logic0) Voltage	-0.3	V_{REF} – 0.125	V	

Note:
1. Inputs are not recognized as valid until VREF stabilizes.
2. VREF is expected to be equal to 0.5 V DDQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed 2% of the DC value.
3. VDDQ tracks with VDD, VDDL tracks with VDD.
4. VTT of transmitting device track VREF of receiving device.

Environmental Parameters

Symbol	Parameter	Rating	Units	Note
T_{OPR}	Module Operating Temperature Range (ambient)	0 to 55	°C	3
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
T_{STG}	Storage Temperature (Plastic)	-55 to 100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

Note:
1. Stresses greater than those listed may cause permanent damage to the device. This is a tress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The component maximum case temperature shall not exceed the value specified in the component spec.

Operating, Standby, and Refresh Currents

T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.8V ± 0.1V (1GB, 1 Rank, 128Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-6400	Unit
I_{DD0}	Operating Current: one bank; active/precharge; T_{rc} = $T_{rc\ (MIN)}$; T_{ck} = $T_{ck\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	616	mA
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; T_{rc} = $T_{rc\ (MIN)}$; CL=2.5; T_{ck} = $T_{ck\ (MIN)}$; I_{OUT} = 0Ma; address and control inputs changing once per clock cycle	748	mA
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; T_{ck} = $T_{ck\ (MIN)}$	79	mA
I_{DD2N}	Idle Standby Current: CS ≥ $V_{IH\ (MIN)}$; all banks idle; CKE ≥ $V_{IH\ (MIN)}$; T_{ck} = $T_{ck\ (MIN)}$; address and control inputs changing once per clock cycle	352	mA
I_{DD2Q}	Precharge Quiet Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; t_{CK} = $t_{CK\ (MIN)}$; Other control and address inputs are stable, Data bus inputs are floating.	308	mA
I_{DD3PF}	Active Power-Down Current: All banks open; T_{ck} = $T_{ck\ (MIN)}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **low** (Fast Power-down Exit).	264	mA
I_{DD3PS}	Active Power-Down Current: All banks open; T_{ck} = $T_{ck\ (MIN)}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **high** (Slow Power-down Exit).	88	mA
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ $V_{IH\ (MIN)}$; CKE ≥ $V_{IH\ (MIN)}$; T_{rc} = $T_{ras\ (MAX)}$; T_{ck} = $T_{ck\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	440	mA
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; T_{ck} = $T_{ck\ (MIN)}$	1056	mA
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; T_{ck} = $T_{ck\ (MIN)}$; I_{OUT} = 0Ma	1056	mA
I_{DD5}	Auto-Refresh Current: T_{rc} = $T_{rfc\ (MIN)}$	1540	mA
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	79	mA
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; T_{rc} = T_{rc} (min); I_{OUT} = 0Ma.	2200	mA
Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.			

Operating, Standby, and Refresh Currents

T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.8V ± 0.1V (2GB, 2 Ranks, 128Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-6400	Unit
I_{DD0}	Operating Current: one bank; active/precharge; T_{RC} = T_{RC} (MIN); T_{CK} = T_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	968	mA
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; T_{RC} = T_{RC} (MIN); CL=2.5; T_{CK} = T_{CK} (MIN); I_{OUT} = 0Ma; address and control inputs changing once per clock cycle	1100	mA
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V_{IL} (MAX); T_{CK} = T_{CK} (MIN)	158	mA
I_{DD2N}	Idle Standby Current: CS ≥ V_{IH} (MIN); all banks idle; CKE ≥ V_{IH} (MIN); T_{CK} = T_{CK} (MIN); address and control inputs changing once per clock cycle	704	mA
I_{DD2Q}	Precharge Quiet Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; t_{CK} = $t_{CK\ (MIN)}$; Other control and address inputs are stable, Data bus inputs are floating.	616	mA
I_{DD3PF}	Active Power-Down Current: All banks open; T_{CK} = T_{CK} (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **low** (Fast Power-down Exit).	528	mA
I_{DD3PS}	Active Power-Down Current: All banks open; T_{CK} = T_{CK} (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **high** (Slow Power-down Exit).	176	mA
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ V_{IH} (MIN); CKE ≥ V_{IH} (MIN); T_{RC} = T_{RAS} (MAX); T_{CK} = T_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	792	mA
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; T_{CK} = T_{CK} (MIN)	1408	mA
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; T_{CK} = T_{CK} (MIN); I_{OUT} = 0Ma	1408	mA
I_{DD5}	Auto-Refresh Current: T_{RC} = T_{RFC} (MIN)	1892	mA
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	158	mA
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; T_{RC} = T_{RC} (min); I_{OUT} = 0Ma.	2552	mA
Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.			

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	PC2-6400		Unit
		Min.	Max.	
Tck	Clock Cycle Time (Average)	2500	8000	ps
Tch	CK high-level width (Average)	0.48	0.52	Tck
Tcl	CK low-level width (Average)	0.48	0.52	Tck
WL	Write command to DQS associated clock edge	RL-1		Nck
Tdqss	Write command to 1st DQS latching transition	-0.25	0.25	Tck
Tdss	DQS falling edge to CK setup time (write cycle)	0.2	-	Tck
Tdsh	DQS falling edge hold time from CK (write cycle)	0.2	-	Tck
Tdqsl,(H)	DQS input low (high) pulse width (write cycle)	0.35	-	Tck
Twpre	Write preamble	0.35	-	Tck
Twpst	Write postamble	0.4	0.6	Tck
Tis	Address and control input setup time	175	-	ps
Tih	Address and control input hold time	250	-	ps
Tipw	Input pulse width	0.6	-	Tck
Tds	DQ and DM input setup time (differential data strobe)	50	-	ps
Tdh	DQ and DM input hold time(differential data strobe)	125	-	ps
Tdipw	DQ and DM input pulse width (each input)	0.35	-	Tck
Tac	DQ output access time from CK/$\overline{CK}$	-400	400	ps
Tdqsck	DQS output access time from CK/$\overline{CK}$	-350	350	ps
Thz	Data-out high-impedance time from CK/$\overline{CK}$	-	tACmax	ps
Tlz(DQS)	DQS low-impedance time from CK/$\overline{CK}$	tACmin	tACmax	ps
Tlz(DQ)	DQ low-impedance time from CK/$\overline{CK}$	$2t_{AC}$ min	t_{AC} max	ps
Tdqsq	DQS-DQ skew (DQS & associated DQ signals)	-	200	ps
Thp	Minimum half clk period for any given cycle; defined by clk high (Tch) or clk low (Tcl) time	Min(Tch(abs), Tcl(abs))	-	ps
Tqhs	Data hold Skew Factor	-	300	ps
Tqh	Data output hold time from DQS	Thp – Tqhs	-	ps
Trpre	Read preamble	0.9	1.1	Tck
Trpst	Read postamble	0.4	0.6	Tck
Trrd	Active bank A to Active bank B command	7.5	-	ns
Tfaw	Four Activate Window for 1KB page size products	35	-	ns
Tccd	$\overline{CAS}$ to $\overline{CAS}$	2		Nck
Twr	Write recovery time without Auto-Precharge	15	-	ns
Tdal	Auto precharge write recovery + precharge time	WR+tnRP	-	Nck
Twtr	Internal write to read command delay	7.5	-	ns
Trtp	Internal read to precharge command delay	7.5		ns
Tcke	CKE minimum pulse width	3		Nck
Txsnr	Exit self refresh to a Non-read command	Trfc+10		ns
Txsrd	Exit self refresh to a Read command	200		Nck
Txp	Exit precharge power down to any Non- read command	2	-	Nck

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

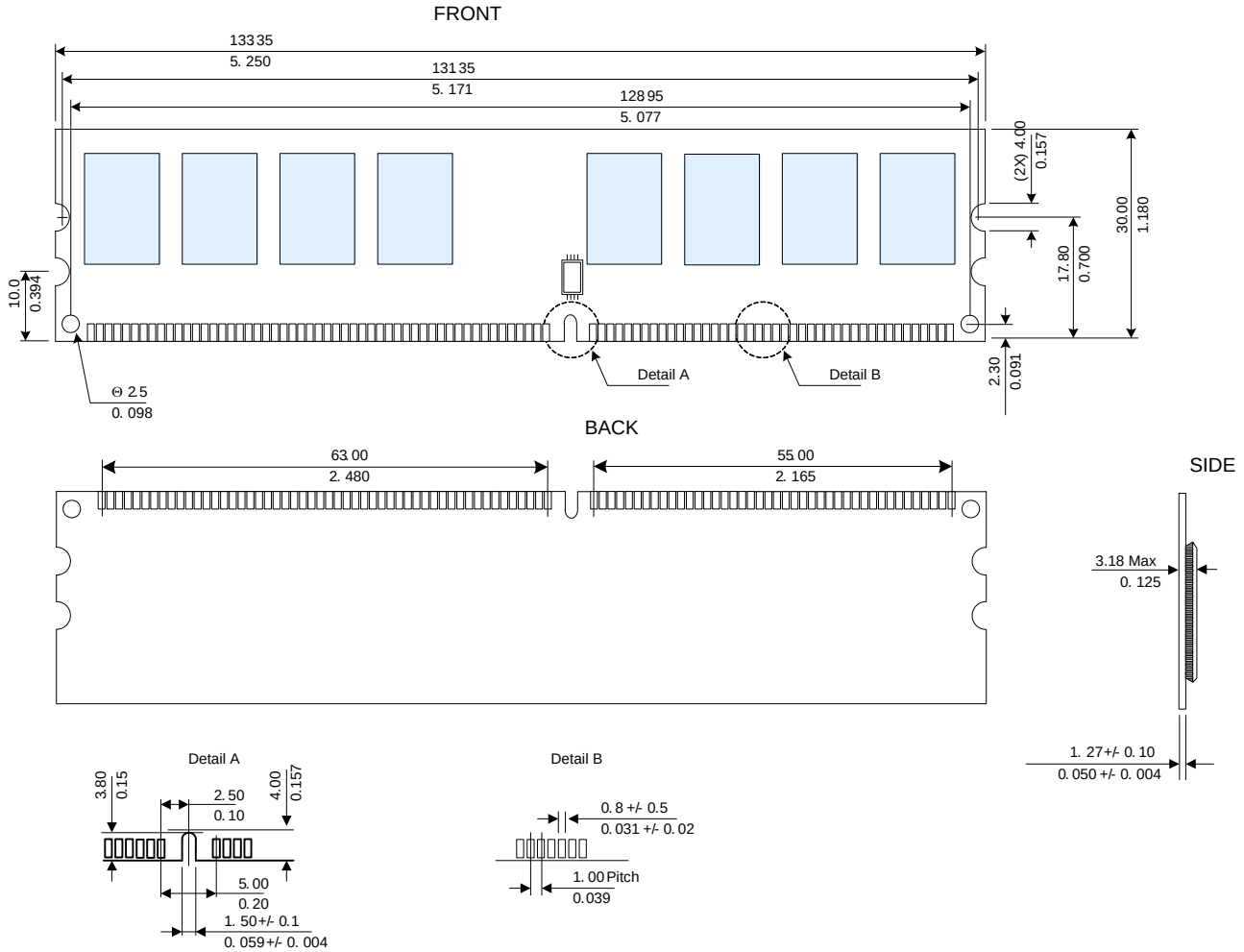
Symbol	Parameter	PC2-6400		Unit
		Min.	Max.	
Txard	Exit active power down to read command	2	-	Nck
Txards	Exit active power down to read command	8-AL		Nck
Taond	ODT turn-on delay	2	2	Nck
Taon	ODT turn-on	Tac (min)	Tac (max)+0.7	ns
Taonpd	ODT turn-on (Power down mode)	Tac (min) +2	2Tck + Tac(max) +1	ns
Taofd	ODT turn-off delay	2.5	2.5	Nck
Taof	ODT turn-off	Tac(min)	Tac(max) +0.6	ns
Taofpd	ODT turn-off (Power down mode)	Tac (min)+2	2.5Tck + Tac(max) +1	ns
Tanpd	ODT to power down entry latency	3	-	Nck
Taxpd	ODT power down exit latency	8		Nck
Tmrd	Mode register set command cycle time	2	-	Nck
Tmod	MRS command to ODT update delay	0	12	ns
Toit	OCD drive mode output delay	0	12	ns
tDelay	Minimum time clocks remains ON after CKE asynchronously drops Low	Tis + Tck + Tih	-	ns
Trfc	Refresh to active/Refresh command time	127.5		ns
Trefi	Average Periodic Refresh Interval (85ºC < T_{CASE} ≤ 95ºC)	3.9		µs
	Average Periodic Refresh Interval (0ºC ≤ T_{CASE} ≤ 85ºC)	7.8		µs

Speed Grade Definition

Symbol	Parameter	PC2-6400		Unit
		Min	Max	
Tras	Row Active Time	45	70,000	ns
Trc	Row Cycle Time	57.5	-	ns
Trcd	RAS to CAS delay	12.5	-	ns
Trp	Row Precharge Time	12.5	-	ns

Package Dimensions

(Raw Card Version: D, 1GB, 1 Rank, 128Mx8 DDR2 SDRAMs)

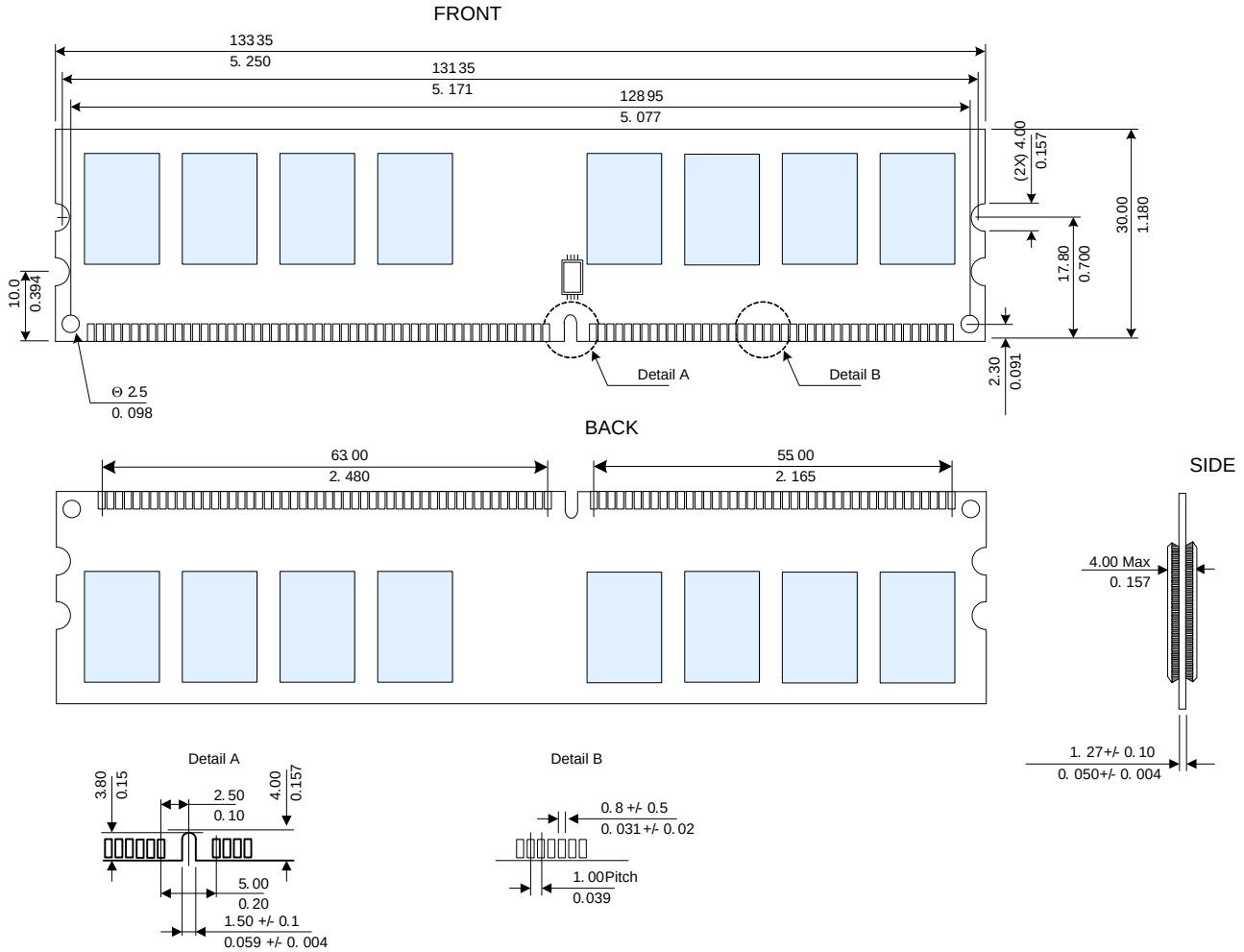


Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated

Units: Millimeters (Inches)

Package Dimensions

(Raw Card Version: E, 2GB, 2 Ranks, 128Mx8 DDR2 SDRAMs)



Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated

Units: Millimeters (Inches)

Revision Log

Rev	Date	Modification
0.1	01/2010	Preliminary Edition
1.0	10/2010	Official Release